REMARKS

In this response, Applicants amend Claim 28. Applicants do not cancel or add any claims. Accordingly, Claims 20-29 are pending.

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attachment is captioned "Version With Markings To Show Changes Made."

Applicants note that the amendment to Claim 28 is not being made to overcome any rejection or prior art or for any reason related to a statutory requirement for patentability. Rather, Applicants make the amendment merely to place Claim 28 in a format that is more consistent with the other pending claims.

Claims Rejected Under 35 U.S.C. § 102(b)

The Patent Office rejects Claims 20-29 under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,477,413 to Watt ("Watt"). Applicants respectfully traverse this rejection.

In order to anticipate a claim, the relied upon reference must disclose every limitation of the claim. Among other limitations, independent Claim 20 recites forming a performance circuit in a first well of a substrate, forming a protection circuit in a second well of a substrate separate from the first well, and coupling the protection circuit to the performance circuit (emphasis added). Applicants submit that Watt fails to disclose all of these limitations.

In making the rejection, the Patent Office relies on Watt to show forming performance circuit 54, 55 that occupies first well 53, forming protection circuit 52 that occupies second well 51, and coupling the protection circuit to the performance circuit (Figure 5). In response, Applicants respectfully disagree with the Patent Office's characterization of the device shown in Figure 5.

Specifically, Watt does not describe reference characters 54, 55 located within well 53 as a performance circuit, as suggested by the Patent Office. Rather, only a cursory review of Watt is necessary to see that nMOSFETs 54 and 55 within p-well 53 form the positive ESD protection component of an ESD protection circuit and diode 52 within p-well 51 forms the negative ESD protection component of the ESD protection circuit (Col. 7, lines 2-9). Therefore, Applicants submit that forming a positive component of a protection circuit in one well of a substrate and

forming the negative component of the protection circuit in a second well within the substrate is not the same as forming a performance circuit in one well of a substrate and forming a protection circuit in a second well of the substrate, as recited in Applicants' independent Claim 20. Thus, at least this limitation is not disclosed by Watt.

Accordingly, Applicants respectfully request withdrawal of the rejection of independent Claim 20. Claims 21-29 depend from independent Claim 20 and contain all of the limitations thereof. Thus, the rejected dependent claims are not anticipated at least for the same reasons as independent Claim 20.

CONCLUSION

In view of the foregoing, it is believed that all claims now pending (1) are in proper form, (2) are neither obvious nor anticipated by the relied upon art of record, and (3) are in condition for allowance. A Notice of Allowance is earnestly solicited at the earliest possible date. If the Examiner believes that a telephone conference would be useful in moving the application forward to allowance, the Examiner is encouraged to contact the undersigned at (310) 207-3800.

If necessary, the Commissioner is hereby authorized in this, concurrent and future replies, to charge payment or credit any overpayment to Deposit Account No. 02-2666 for any additional fees required under 37 C.F.R. §§ 1.16 or 1.17, particularly, extension of time fees.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: 12/11, 2002

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CERTIFICATE OF MAILING:

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail with sufficient postage in an envelope addressed to: Box Non-Fee Amendment, Assistant Commissioner for Patents, Washington, D.C. 20231, on December 11, 2002

Lillian E. Rodriguez 12-11-02

Lillian E. Rodriguez December 11, 2002

VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Please amend the claims as follows:

28. (Amended) The method of claim 27, the doped region being a first doped region of a first dopant in a well of the substrate, the well being doped with a concentration of a second dopant and [the step of] wherein forming a performance circuit further comprises:

forming a source region of the transistor doped with the first dopant in the well separated from the drain region by the gate to form a unit transistor.